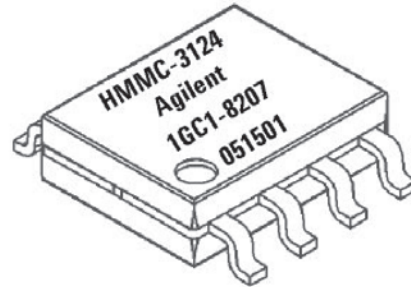


Agilent HMMC-3124 DC-12 GHz Packaged High Efficiency Divide-by-4 Prescaler

HMMC-3124-TR1 - 7" diameter reel/500 each
HMMC-3124-BLK - Bubble strip/10 each
Data Sheet



Description

The HMMC-3124 is a packaged GaAs HBT MMIC prescaler which offers dc to 12 GHz frequency translation for use in communications and EW systems incorporating high-frequency PLL oscillator circuits and signal-path down conversion applications. The prescaler provides a large input power sensitivity window and low phase noise.

Package Type: SOIC-8 Plastic
Package Dimensions: 4.9 x 3.9 mm typ
Package Thickness: 1.55 mm typ
Lead Pitch: 1.25 mm nom
Lead Width: 0.42 mm nom

Features

- **Wide Frequency Range:**
0.2–12 GHz
- **High Input Power Sensitivity:**
On-chip pre- and post-amps
-15 to +10 dBm (1–8 GHz)
-10 to +8 dBm (8–10 GHz)
-5 to +2 dBm (10–12 GHz)
- **P_{out}: 0 dBm (0.5 V_{p-p})**
- **Low Phase Noise:**
-153 dBc/Hz @ 100 kHz Offset
- **(+) or (-) Single Supply Bias Operation**
- **Wide Bias Supply Range:**
4.5 to 6.5 volt operating range
- **Differential I/O with on-chip 50Ω matching**

Absolute Maximum Ratings¹

(@ T_A = +25 °C, unless otherwise stated)

Symbol	Parameters/Conditions	Min	Max	Units
V _{CC}	Bias Supply Voltage		+7	volts
V _{EE}	Bias Supply Voltage	-7		volts
V _{CC} - V _{EE}	Bias Supply Delta		+7	volts
V _{Logic}	Logic Threshold Voltage	V _{CC} - 1.5	V _{CC} - 1.2	volts
P _{in(CW)}	CW RF Input Power		+10	dBm
V _{RFin}	DC Input Voltage (@ RFin or $\overline{\text{RFin}}$ Ports)		V _{CC} ±0.5	volts
T _{BS} ²	Backside Operating Temperature	-40	+85	°C
T _{st}	Storage Temperature	-65	+165	°C
T _{max}	Maximum Assembly Temperature (60 seconds max)		310	°C

Notes:

1. Operation in excess of any parameter limit (except T_{BS}) may cause permanent damage to the device.
2. MTTF > 1 x 10⁶ hours @ T_{BS} ≤ 85°C. Operation in excess of maximum operating temperature (T_{BS}) will degrade MTTF.



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DC Specifications/Physical Properties

($T_A = +25\text{ }^\circ\text{C}$, $V_{CC} - V_{EE} = 5.0$ volts, unless otherwise listed)

Symbol	Parameters/Conditions	Min	Typ	Max	Units
$V_{CC} - V_{EE}$	Operating bias supply difference ¹	4.5	5.0	6.5	volts
$ I_{CC} $ or $ I_{EE} $	Bias supply current	34	40	46	mA
$V_{RFIn(q)}$ $V_{RFout(q)}$	Quiescent dc voltage appearing at all RF ports		V_{CC}		volts
V_{Logic}	Nominal ECL Logic Level (V_{Logic} contact self-bias voltage, generated on-chip)	$V_{CC} - 1.45$	$V_{CC} - 1.32$	$V_{CC} - 1.25$	volts

Notes:

1. Prescaler will operate over full specified supply voltage range. V_{CC} or V_{EE} not to exceed limits specified in Absolute Maximum Ratings section.

RF Specifications

($T_A = +25\text{ }^\circ\text{C}$, $Z_0 = 50\ \Omega$, $V_{CC} - V_{EE} = 5.0\text{ volts}$)

Symbol	Parameters/Conditions	Min	Typ	Max	Units
$f_{in(max)}$	Maximum input frequency of operation	12	14		GHz
$f_{in(min)}$	Minimum input frequency of operation ¹ ($P_{in} = -10\text{ dBm}$)		0.2	0.5	GHz
$f_{Sel-Osc.}$	Output Self-Oscillation Frequency ²		3.4		GHz
P_{in}	@ dc, (Square-wave input)	-15	>-25	+10	dBm
	@ $f_{in} = 500\text{ MHz}$, (Sine-wave input)	-15	>-20	+10	dBm
	$f_{in} = 1\text{ to }8\text{ GHz}$	-15	>-20	+10	dBm
	$f_{in} = 8\text{ to }10\text{ GHz}$	-10	>-15	+5	dBm
	$f_{in} = 10\text{ to }12\text{ GHz}$	-5	>-10	-1	dBm
RL	Small-Signal Input/Output Return Loss (@ $f_{in} < 10\text{ GHz}$)		15		dB
S_{12}	Small-Signal Reverse Isolation (@ $f_{in} < 10\text{ GHz}$)		30		dB
φ_N	SSB Phase noise (@ $P_{in} = 0\text{ dBm}$, 100 KHz offset from a $f_{out} = 1.2\text{ GHz}$ Carrier)		-153		dBc/Hz
Jitter	Input signal time variation @ zero-crossing ($f_{in} = 10\text{ GHz}$, $P_{in} = -10\text{ dBm}$)		1		ps
T_r or T_f	Output transition time (10% to 90% rise/fall time)		70		ps
P_{out}^3	@ $f_{out} < 1\text{ GHz}$	-2.0	0.0		dBm
	@ $f_{out} = 2.5\text{ GHz}$	-3.5	-1.5		dBm
	@ $f_{out} = 3.0\text{ GHz}$	-4.5	-2.5		dBm
$ V_{out(p-p)} ^4$	@ $f_{out} < 1\text{ GHz}$		0.5		volts
	@ $f_{out} = 2.5\text{ GHz}$		0.42		volts
	@ $f_{out} = 3.0\text{ GHz}$		0.37		volts
$P_{Spitback}$	f_{out} power level appearing at \overline{RF}_{in} or \overline{RF}_{out} (@ $f_{in} = 10\text{ GHz}$, Unused RF_{out} or \overline{RF}_{out} unterminated)		-50		dBm
	f_{out} power level appearing at \overline{RF}_{in} or \overline{RF}_{out} (@ $f_{in} = 10\text{ GHz}$, Both RF_{out} or \overline{RF}_{out} unterminated)		-55		dBm
$P_{feedthru}$	Power level of f_{in} appearing at RF_{out} or \overline{RF}_{out} (@ $f_{in} = 12\text{ GHz}$, $P_{in} = 0\text{ dBm}$, Referred to $P_{in}(f_{in})$)		-30		dBc
H_2	Second harmonic distortion output level (@ $f_{out} = 3.0\text{ GHz}$, Referred to $P_{out}(f_{out})$)		-25		dBc

Notes:

- For sine-wave input signal. Prescaler will operate down to dc for square-wave input signal. Min. divide frequency limited by input slew rate.
- Prescaler can exhibit this output signal under bias in the absence of an RF input signal. This condition can be eliminated by use of the Input dc offset technique described on page 4.
- Fundamental of output square wave's Fourier Series.
- Square wave amplitude calculated from P_{out} .

Applications

The HMMC-3124 is designed for use in high frequency communications, microwave instrumentation, and EW radar systems where low phase-noise PLL control circuitry or broad-band frequency translation is required.

Operation

The device is designed to operate when driven with either a single-ended or differential sinusoidal input signal over a 200 MHz to 12 GHz bandwidth. Below 200 MHz the prescaler input is “slew-rate” limited, requiring fast rising and falling edge speeds to properly divide. The device will operate at frequencies down to dc when driven with a square-wave.

Due to the presence of an off-chip RF-bypass capacitor inside the package (connected to the V_{CC} contact on the device), and the unique design of the device itself, the component may be biased from either a single positive or single negative supply bias. The backside of the package is not dc connected to any dc bias point on the device.

For positive supply operation, V_{CC} pins are nominally biased at any voltage in the +4.5 to +6.5 volt range with pin 8 (V_{EE}) grounded. For negative bias operation V_{CC} pins are typically grounded and a negative voltage between -4.5 to -6.5 volts is applied to pin 8 (V_{EE}).

ac-Coupling and dc-Blocking

All RF ports are dc connected on-chip to the V_{CC} contact through on-chip 50Ω resistors. Under any bias conditions where V_{CC} is not dc grounded the RF ports should be ac coupled via series capacitors mounted on the PC-board at each RF port. Only under bias conditions where V_{CC} is dc grounded (as is typical for negative bias supply operation) may the RF ports be direct coupled to adjacent circuitry or in some cases, such as level shifting to subsequent stages. In the latter case the package heat sink may be “floated” and bias applied as the difference between V_{CC} and V_{EE} .

Input dc Offset

If an RF signal with sufficient signal to noise ratio is present at the RF input lead, the prescaler will operate and provide a divided output equal the input frequency divided by the divide modulus. Under certain “ideal” conditions where the input is well matched at the right input frequency, the component may “self-oscillate”, especially under small signal input powers or with only noise present at the input. This “self-oscillation” will produce an undesired output signal also known as a false trigger. To prevent false triggers or self-oscillation conditions, apply a 20 to 100 mV dc offset voltage between the RF_{in} and RF_{in} ports. This prevents noise or spurious low level signals from triggering the divider.

Adding a $10K\Omega$ resistor between the unused RF input to a contact point at the V_{EE} potential will result in an offset of $\approx 25mV$ between the RF inputs. Note, however, that the input sensitivity will be reduced slightly due to the presence of this offset.

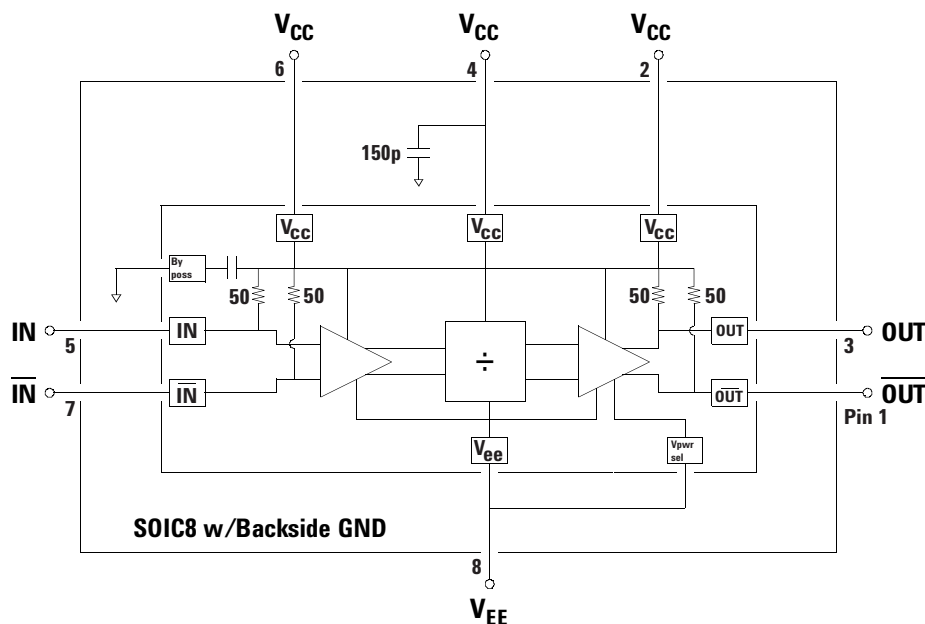


Figure 1. Simplified Schematic

Supplemental Data

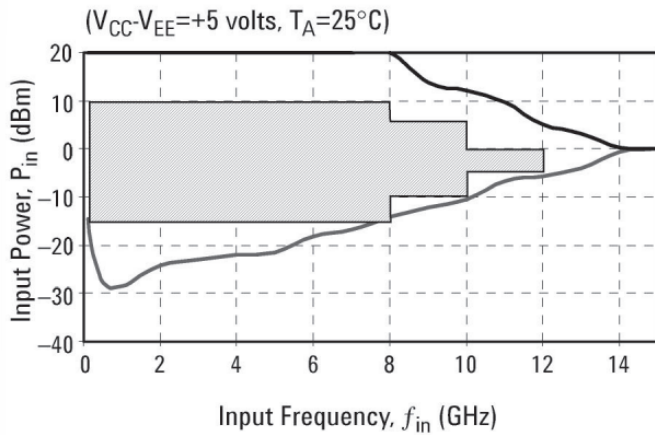


Figure 4. Typical Input Sensitivity Window

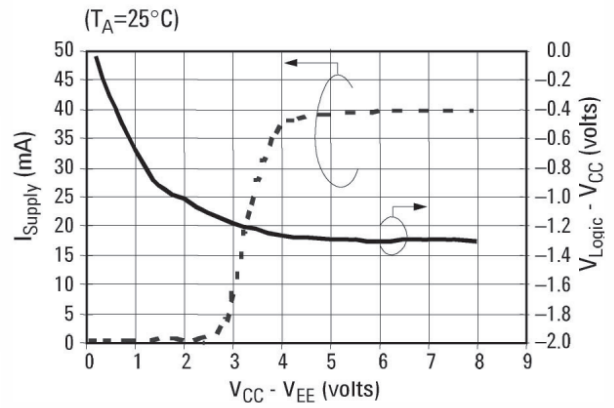


Figure 5. Typical Supply Current & V_{Logic} vs. Supply Voltage

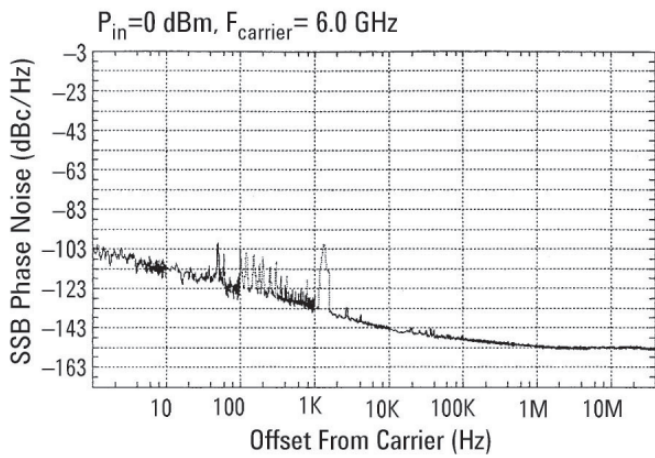


Figure 6. Typical Phase Noise Performance

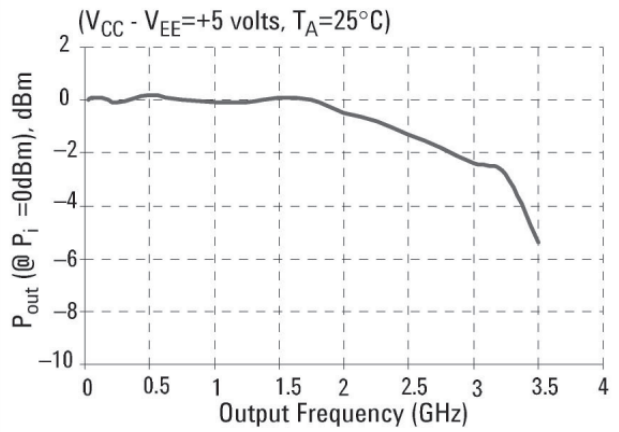


Figure 7. Typical Output Power vs. Output Frequency f_{out} (GHz)

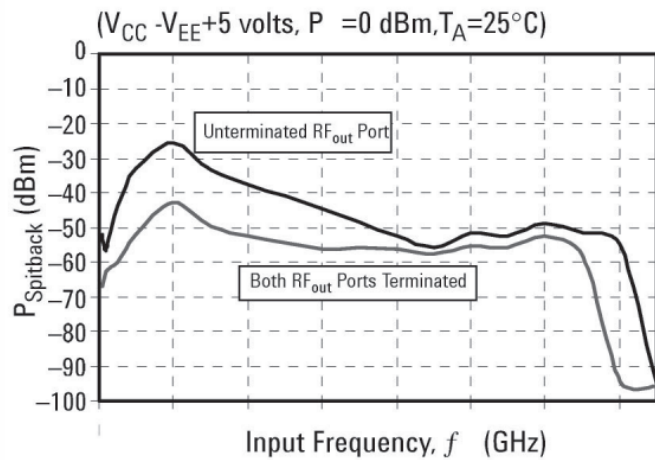
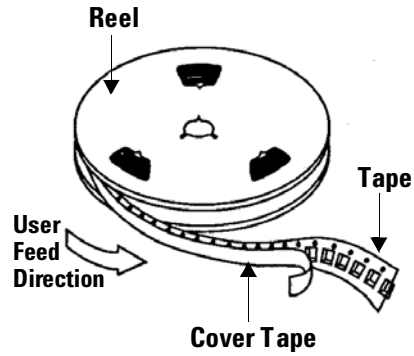
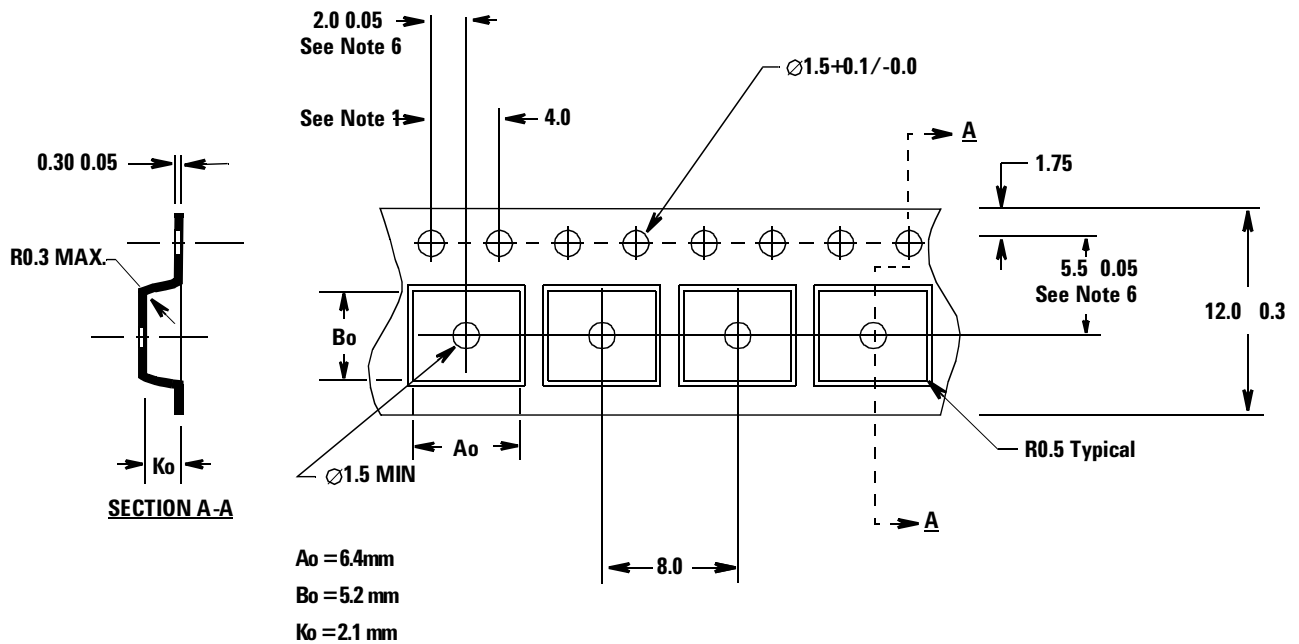


Figure 8. Typical "Spitback" Power ($P_{f_{out}}$) appearing at RF input port

Device Orientation



Tape Dimensions and Product Orientation



Notes:

1. 10 sprocket hole pitch cumulative tolerance: 0.2mm.
2. Camber not to exceed 1mm in 100mm.
3. Material: Black Conductive Advantek Polystyrene.
4. A_o and B_o measured on a plane 0.3mm above the bottom of the pocket.
5. K_o measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

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